a power transistor connected between a second node connected to the second transmission line and an output node of the voltage regulator; and

a switch circuit configured to select a level of a gate voltage supplied to a gate of the power transistor and a level of a body voltage supplied to a body of the power transistor in response to a first power sequence of the first voltage, a second power sequence of the second voltage, and an operation control signal.

14. The mobile device of claim **13**, wherein the error amplifier comprises:

an amplifier stage having a two-stage cascode architecture and configured to amplify the difference between the reference voltage and the feedback voltage; and

an output stage having a two-stage cascode architecture and configured to output the amplified voltage from the amplifier stage to the switch circuit.

15. The mobile device of claim **14**, wherein the output stage comprises:

a first feedback loop disposed at a pull-up path between the first node and an output node of the error amplifier; and

a second feedback loop disposed at a pull-down path between the output node of the error amplifier and a ground.

16. The mobile device of claim **13**, wherein the switch circuit comprises:

a first switch circuit connected between an output node of the error amplifier and the gate of the power transistor;

a second switch circuit connected to the first node, the second node, and the gate of the power transistor; and

a third switch circuit connected to the first node, the second node, and the body of the power transistor.

17. The mobile device of claim **16**, wherein the first switch circuit controls a connection between the output node of the error amplifier and the gate of the power transistor in response to a power-on signal generated in response to the first power sequence and the second power sequence, the second switch circuit controls a connection between the first node and the gate of the power transistor and a connection between the second node and the gate of the power transistor in response to the power-on signal and the operation control signal, and the third switch circuit controls a connection between either of the first and second nodes and the body of the power transistor in response to the power-on signal and the operation control signal.

18. A mobile device, comprising:

a memory;

a memory controller comprising a voltage regulator; and

a power management integrated circuit configured to supply a first voltage and a second voltage to the voltage regulator and to supply a third voltage to the memory,

wherein the voltage regulator comprises:

an error amplifier configured to receive the first voltage through a first node as an operating voltage, to amplify a difference between a reference voltage and a feedback voltage, and to output an amplified voltage;

a power transistor connected between a second node receiving the second voltage and an output node of the voltage regulator; and

a switch circuit configured to select a level of a gate voltage supplied to a gate of the power transistor and a level of a body voltage supplied to a body of the power transistor in response to a first power sequence of the first voltage, a second power sequence of the second voltage, and an operation control signal, and

the first voltage is higher than the second voltage.

19. The mobile device of claim **18**, wherein the error amplifier comprises:

an amplifier stage having a two-stage cascode architecture and configured to amplify the difference between the reference voltage and the feedback voltage; and

an output stage having the two-stage cascode architecture and configured to output the amplified voltage from the amplifier stage to the switch circuit.

20. The mobile device of claim **19**, wherein the switch circuit comprises:

a first switch circuit connected between an output node of the error amplifier and the gate of the power transistor;

a second switch circuit connected to the first node, the second node, and the gate of the power transistor; and

a third switch circuit connected to the first node, the second node, and the body of the power transistor.

21-25. (canceled)

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